D.3: Timing and Tracking for the CB Detector

Timing and Trigger-Signal Processing

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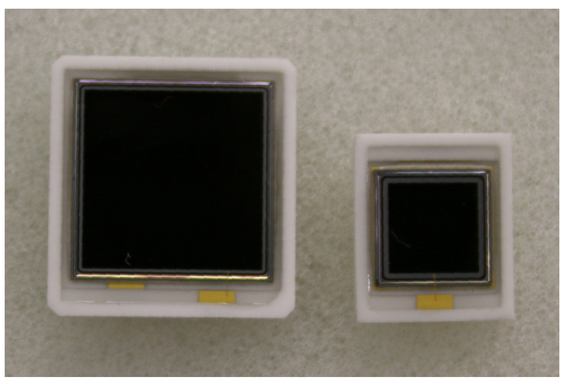
Motivation:

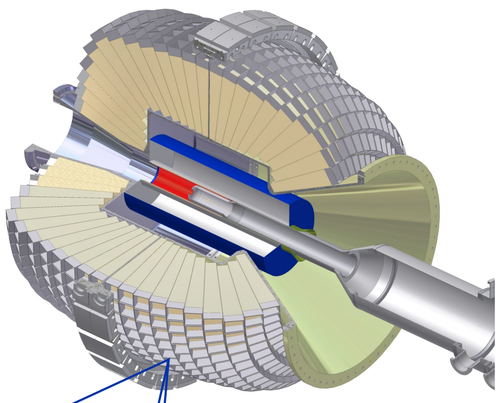
The Crystal Barrel detector is well suited to identify photo-production reactions with neutral particles final states. The read-out of the calorimeter is done using photo-diodes providing a high quality energy information. In order to suppress noise from the photo-diodes, a charge sensitive pre-amplifier is used. This yields a rise time of 2.5 μs and a decay time of 100 μs as shape of the primary signal. The width of the signal causes a time stability that is in the vicinity of 100 ns which is too much for the next generation trigger timing demands. Therefore, a new read-out equipment for the CsI(Tl) detectors of the Crystal Barrel detector is planned using making of avalanche photo-diodes (APDs).

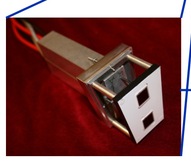


APD Hamamatsu S8664-1010SPL which is used in the test setup.

3x3 CsI(Tl) test array equipped with Hamamatsu APDs.

Planned Modification for the Crystal Barrel Detector:

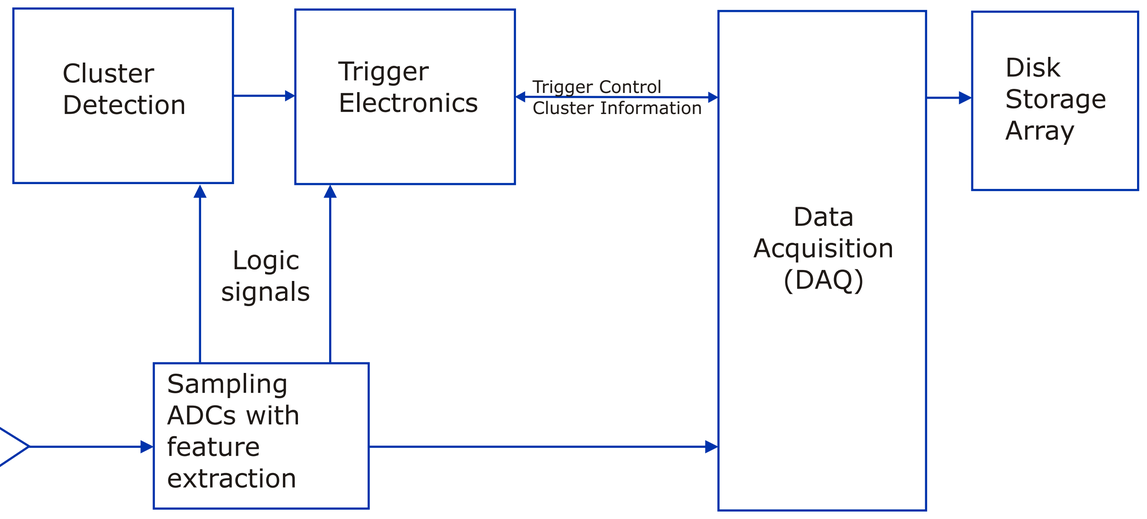




CsI(Tl) detectors equipped with APDs.

1440 Channels

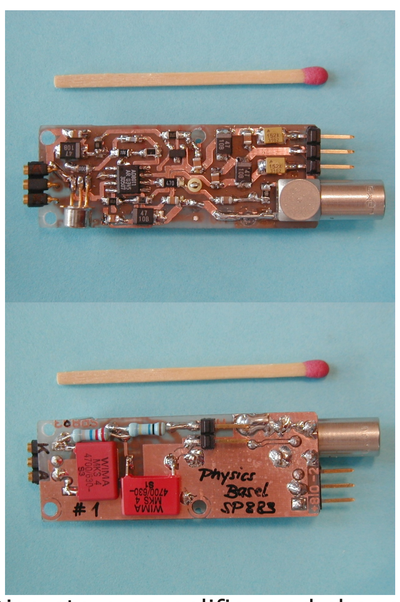
Preamplifier installed in the hats.



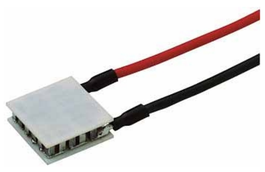
- CsI(Tl) read-out via APDs,
- High integrated (ASICs) preamplifiers and shaping electronics,
- Sampling ADC with feature extraction as
  - timing,
  - energy deposit,
  - event based pedestal subtraction.
- High speed FPGA cluster, finder for first level triggering,
- Multipurpose FPGA trigger, system,
- Fiber optics read-out and synchronization,
- Performant data acquisition based on parallelized read-out,
- Disk storage Array and Archive system (Sun SAM-FS),
- Redundant storage in computer cluster using LUSTRE file system.

First Test Setup:

Test setup with 3x3 CsI(Tl) crystal array.



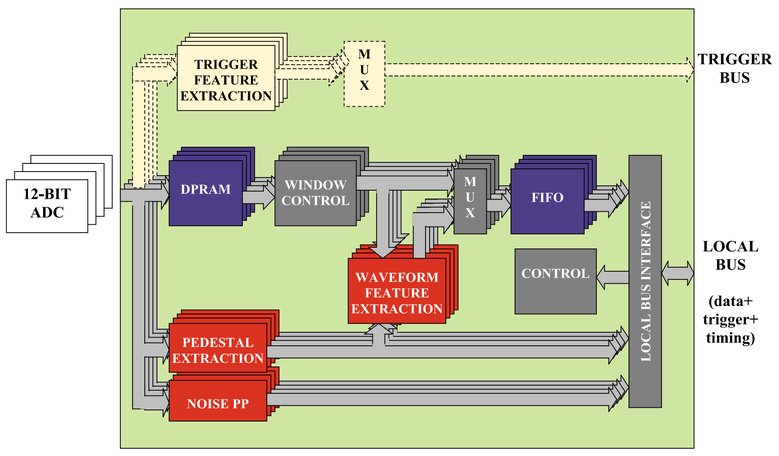
Discrete preamplifier and shaper.



Peltier element.

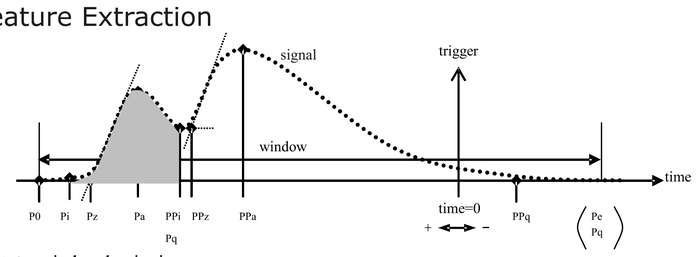
- Tests with photon beam,
  Results see D.3: New read-out for CsI(Tl) crystals,
- Evaluate different designs of:
  - Preamplifier,
  - Shaper,
  - APD arrangement.
- Study temperature dependence of APDs and electronics, temperature stabilization using Peltier elements.

Sampling ADCs with Trigger Signal Processing:



Flow plan of a sampling ADC with feature extraction (design: P. Marcinewski).

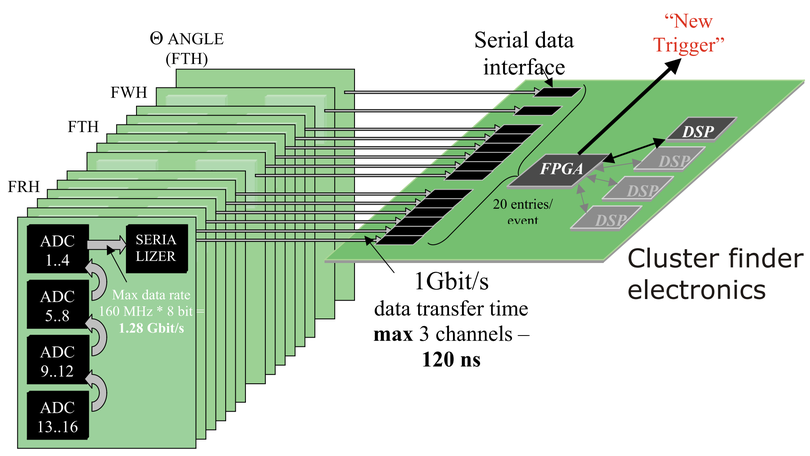
Feature Extraction



P0 –window beginning
Pi – time for the first non-zero value
Pz – pulse start time calculated from slope crossing the pedestal value
Pa – signal amplitude
Pq – signal integral (charge) *

PPi – minimum value before pileup
PPz – pileup pulse start time calculated from slope crossing the momentary pedestal value Ppi
PPa – pileup pulse amplitude
Pe – pileup integral, starting from PPi

* If pileup occurs, the integral **Pq** is only calculated untill PPi time



Cluster finder using high-speed FPGAs.